

Cosmic Rays and Microprocessor Vulnerability

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Sources

Cosmic ray info from the following sources:

- Narayan and Xie. “Computing in the Presence of Soft Errors” Asplos 2004.
- Aton, Seitchill, and Schichijo. “Comparison of Charge Collections from Energetic Ions Typical of Neutron-Recoil Events with Charge Collections from Alpha Particle Strikes” 1996.
- May and Woods. “Alpha-particle Induced Soft Errors in Dynamic Memories”. IEEE Transaction on Electronic Devices, Jan 1979.
- Ziegler et al. “Terrestrial Cosmic Rays and Soft Errors”. IBM Journal of Research and Development, 1996.

Kinds of Errors in Systems

- Signal Integrity
- Thermal
- Power Supply Noise
- Substrate Noise
- “Soft Errors”

Soft Errors

- Excess Charge Carries induced by radiation
- Circuit is usually not permanently damaged
- Sometimes called an SEU (“Single Event Upset”)

Types of Radiation

Neutrons

- Generally come from cosmic rays
- Can cause “silicon-recoil”
- Can cause ^{10}B atom to fission into ^7Li and an alpha Particle

Alpha Particles

- Generally come from radioactive decay
- Can cause ionization errors

Cosmic Rays

- Scientists still unsure where they come from
- Most go through a series of collisions with the atmosphere, creating numerous exotic particles. In general only neutrons make it to the ground.
- The sun produces cosmic rays, but they are low energy and they rarely make it to the surface.

Shielding

- For neutrons, 3 feet of concrete reduces flux by 50%.
- Alpha particles much easier to stop (paper is thick enough) but most problems come from radioactive elements in the chip itself.

Anecdotes #1

“May and Woods Incident”

- First widely reported radiation problems (1979)
- Intel 2107 16KBit DRAM chips
- Problem traced to new ceramics packaging facility getting water just downstream from Uranium mine.

Anecdotes #2

Lost Trailer

- In 1985 IBM was worried about problem, was trying to relocate instruments used in seminal 1965-1968 “Quite Sun Years” study.
- After months of searching (people involved all retired or dead) the 17-ton trailer located on a mountainside in Hawaii.
- Equipment still worked, and used to gather readings at various altitudes.

Anecdotes #3

“Hera Problem”

- IBM having issues with errors in “Hera” memory chip.
- After much searching ^{210}Po contamination found.
- After much, much more searching turns out that bottle-cleaning equipment was ionizing air with the isotope to clear acid bottles of dust. The bottles held acid used in chip fabrication.

Anecdotes #4

Sun e-cache problem

- Sun's UltraSPARC-II did not have ECC on the L2 cache for speed reasons.
- Especially on the 8MB enterprise servers, way higher than normal crash rates
- Most likely cause determined to be cosmic rays.
- Sun lost customers

Electrical Engineering Digression

Hardware Mitigation

Hardware Solutions

Process Improvements

- Use doping less susceptible to Boron fission
- Use solder with lower radioactive isotopes
- Silicon-on-Insulator
- Double-gate Devices (redesign of transistors to have two gates. Harder to make)

Hardware Solutions

Circuit Techniques

- Increase the capacitance of state holding nodes. The more charge stored, the harder to flip. But slower.
- “Selective Node Engineering”. Find the paths that are most critical and harden them. Next to no performance penalty, minimal power penalty.
- Adding more transistors at half the size. Gives same performance, but having one flipped won't flip whole circuit.
- Redundant logic, with a vote.
- Have circuits handle glitches better.

Hardware Solutions

Memory Techniques

- ECC Codes
- Memory interleave. Spread bits out, so one big hit is unlikely to flip two adjacent bits in same word.
- Memory scrubbing. . . periodically going through memory and fixing single bit errors before turn into double bit errors.

Some Related Papers

Pentium Investigation

- David M. Hiemstra and Allan Baril. “Single event upset characterization of the Pentium MMX and Pentium II microprocessors using proton irradiation”, IEEE Transactions on Nuclear Science, 1999.
- Experiments were done on off-the-shelf Intel chips to see their resistance to proton radiation.
- Proton radiation was used. Can be done in air (so no need for heat sink). No need to trim off lid of chip (difficult for commercial chips), the facility cost is lower.
- Only the CPU tested. Rest of motherboard shielded by 2 inches of lead
- Bombarded from bottom, to avoid attenuation by heat sink.

Pentium Investigation

Testing Methodology

- Primary test was a DOS program operating directly on hardware.
- Windows test was to run a benchmark under NT, and watch for a Blue Screen of Death!
- Irradiation facility at UBC (University of British Columbia)
- Tested various operation modes, with both cache on and off

Pentium Investigation

Results for Pentium MMX

- Various error modes, from freeze, to blue screen, to self-reboot.
- No power-supply glitches or latchup were caused.
- Under DOS, 85.7% Program Hangs, 14.3% Cache Data Errors. No register, ALU, or FPU errors were detected.
- Estimated upset rate for space shuttle operation would be 0.00129/day

Pentium Investigation

Results for Pentium II

- Various error modes, from freeze, to blue screen, to self-reboot.
- No power-supply glitches or latchup were caused.
- Under DOS, 57.1% Program Hangs, 14.3% L1 Cache Data Errors (double bit as PII has ECC in L1) and 3.6% Calculation errors. No register errors detected.
- Estimated upset rate for space shuttle operation would be 0.00129/day
- Supports retry on in-flight data corruption, may explain some slowdown they noticed with WinNT tests.

Pentium Investigation

Conclusions

- MMX's upset cross-section nearly one-tenth of PII.
- Neither showed tendency to latchup, unlike K5. Latchup is considered unacceptable in space applications.
- Both were irradiated with equivalent of 10 years exposure.
- MMX on space shuttle would upset once every 775 days, the PII once every 83 days.

The CRC ARGOS Project

- Philip J. Shirvani and Edward J. McCluskey. “Fault-Tolerant Systems in a Space Environment - The CRC ARGOS Project”, 1998. (Stanford)
- Equivalent space hardened and off-the-shelf MIPS R3000 chips sent into space in 1999. Operating on the same input data, idea is to see how the two compare.
- Compare hardware based fault tolerance versus software based.
- Also some FPGA experiments
- Status: No information has been updated since 2000. The probe only was supposed to have a 3 year life, strange no results have been published.

Software-Implemented Fault Injection

- Raphael R. Some, Won S. Kim, Garen Khanoyan, Leslie Callum, Anil Agarwal and John J. Beahan. “A Software-implemented Fault Injection Methodology for Design and Validation of System Fault Tolerance”, IEEE 2001.
- Idea: want to put an MPI system in space, but want to use off-the-shelf hardware due to cost.
- To test this, need to test. They propose using software fault injection.

Software-Implemented Fault Injection

Four approaches to fault injection:

- Hardware implemented
- Simulation
- Software implemented
- Hybrid

Software-Implemented Fault Injection

They propose JIFI (JPL's Implementation of a Fault Injector), a Software Implemented Fault System

- The claim software implemented have lower complexity, reduced development effort, lower cost, and increased portability.
- JIFI is application-level software based injector.
- Developed on PowerPC Linux, moved to LynxOS.
- Trigger points added to the source code.

- Supports both time-triggered random faults and location triggered targeted faults.
- Only supports user area faults, not OS level ones.
- Results